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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/814,426
Filing Date: March 31, 2004
Appellant(s): MATTHEWS ET AL.

Robert J. Crawford (32122)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/30/2008 appealing from the Office action mailed March 17, 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments after Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US6963626	Shaeffer et al	11-08-2005
US6738845	Hadwiger et al	05-18-2004

(9) Claim Rejections - 35 USC § 103

Claims 1 –56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shaeffer et al (US6963626) hereinafter Shaeffer in view of Hadwiger et al (US6738845) hereinafter Hadwiger.

As to claims 1, 21, 26, 38, 42, 49, and 53 Shaeffer discloses a communication apparatus, method, and phone comprising: a radio frequency (RF) circuit for operating on a radio frequency signal; and a digital processing circuit coupled to the RF circuit, wherein the digital processing circuit includes:

a first bus master coupled to a bus (Figure 1 illustrates a processor comprising a bus master 12 coupled to a bus that couples memory 118 with processor 116, COL. 5, lines 46 - 63);

wherein accesses by the one or more other bus masters to the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF circuit (Figure 1, time controller 110 is access controller to prevent noise coupling between the analog and digital circuitry, COL. 6, lines 1 - 10);

wherein accesses by the one or more other bus masters to the bus are restricted during a second period of operation in response to a signal asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing

circuit (Time controller 110 comprises a programmed timer that restricts access by shutting down the clocking system via a delay locked loop, COL. 6, lines 10 - 17) .

Shaeffer does not explicitly disclose one or more other bus masters coupled to the bus; and configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters.

However, Hadwiger teaches one or more other bus masters coupled to the bus, and a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters as system illustrated in figure 2. Said figure comprises multiples bus masters such as 201 and 202 with arbiter 211 that configures the common bus access between said masters, (COL. 4, lines 32 - 54).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the processor of Shaeffer with the multiple processor core of Hadwiger to provide a cost effective solution for mobile phones that requires multiple processors, COL. 1, lines 25 - 40. One of ordinary skill in the art would have been motivated to modify the processor of Shaeffer with the multiple processor core of Hadwiger to provide a cost effective solution for mobile phones that requires multiple processors, COL. 1, lines 25 - 40.

Hadwiger teaches wherein the bus arbiter is further configured to implement a less favorable arbitration policy for the one or more other bus masters in response to a signal indicating a change to an active mode of operation of the RF circuit (Figure 3 illustrates an arbiter 211 that comprises three arbiters, namely 314,315, and 316. The programmable arbitration priority is set dependent on the bandwidth requirement of

subsystem. The system comprises of 15 programmable slots in a round robin-table. System that is at the bottom of the programmable slots would have a less favorable arbitration policy, COL. 9, lines 1 – 30).

As to claims 2,23, and 27, are Shaeffer discloses the communication apparatus wherein the signal is indicative of a change to an active mode of operation of the RF circuit (Figure 7A illustrates the mode change from analog to digital, COL. 9, lines 27 - 39).

As to claim 3, Shaeffer discloses the communication apparatus wherein the signal indicates a change to a transmission mode of operation of the RF circuit (Figure 3 illustrates transmission mode from analog front end to digital circuitry, COL. 8, lines 1 - 10).

As to claim 4, Shaeffer discloses the communication apparatus as recited in claim 2 wherein the signal indicates a change to a reception mode of operation of the RF circuit (Figure 4 illustrates reception mode from digital circuitry to analog, COL. 8, lines 12 - 23).

As to claims 5, 28, 24, 34, and 43 Shaeffer discloses the communication apparatus wherein the signal is asserted a predetermined amount of time prior to the change to

the active mode of operation of the RF circuit (Said limitation illustrated in Figure 7C, COL. 9, lines 40 - 50).

As to claims 6, 29,35,40,51 Shaeffer discloses the communication apparatus wherein the signal is asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit (Said limitation is illustrated in Figure 7D, COL. 9, lines 45 - 50).

As to claims 7,30, 36, and 55, Shaeffer discloses the communication apparatus wherein the signal indicative of a change of mode of operation of the RF circuit is generated by a timing circuit (Figure 1 illustrates said timing circuit, timing controller 110, Col. 5, lines 46 - 63).

As to claims 8,25,31,37, 39, and 44 Hadwiger discloses the communication apparatus wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal (When the first bus master assets control, it has exclusive access, page 4, paragraph 0044).

As to claims 9, and 45 Hadwiger discloses the communication apparatus wherein the first bus master is a microcontroller unit (MCU) (said limitation is depicted in figure 2, page 2, paragraph 0023).

As to claim 10, Hadwiger discloses the communication apparatus wherein the first bus master is a digital signal processor (DSP) (said limitation is depicted in figure 2, page 2, paragraph 0023).

As to claim 11, Hadwiger discloses the communication apparatus wherein an interrupt signal is provided to the MCU and wherein an interrupt service routine executed by the MCU in response to assertion of the interrupt signal is performed when accesses by masters other than the first bus master to the bus are restricted (Said limitation, page 4, paragraph 0044).

As to claim 12, Hadwiger discloses the communication apparatus wherein the interrupt service routine performs functionality to prepare the digital processing circuit for a shutdown mode of the digital processing circuit (Said limitation, page 4, paragraph 0044).

As to claim 13, Hadwiger discloses the communication apparatus wherein the bus is a multi-layer bus, wherein the first bus master is provided exclusive access to one layer of the bus in response to assertion of the signal while the one or more other bus masters are allowed access to another layer of the multi-layer bus (Multiple arbitration systems and buses are present to afford access to other bus system concurrently, page 2, paragraph 0023).

As to claims 14, and 51, Shaeffer discloses the communication apparatus wherein the shutdown mode of operation includes disabling at least a portion of the digital processing circuit (Figure 1 illustrates time controller disabling digital circuit 116, COL. 6, lines 5 - 10).

As to claim 15, 41, and 52, Shaeffer discloses the communication apparatus wherein the shutdown mode of operation includes disabling a clock that clocks at least a portion of the digital processing circuit (PLL or DLL controls clock, COL. 6, lines 10 - 17).

As to claim 16, Hadwiger discloses the communication apparatus wherein the bus arbiter is configured to restrict the granting of ownership of the bus to the one or more other bus masters in response to the signal (The arbiter module BAM of figure 2 dictates bus ownership, page 1, paragraph 0010).

As to claim 17, Hadwiger discloses the communication apparatus wherein the one or more other bus masters are configured to inhibit requests to gain ownership of the bus in response to the signal (The arbiter module BAM of figure 2 dictates bus ownership, page 1, paragraph 0010).

As to claim 18, 22, 46, and 56 Hadwiger discloses the communication apparatus wherein accesses by the one or more other bus masters are restricted by implementing a less favorable arbitration policy for the one or more other bus masters in response to

the signal (The arbitration module is programmed to afford less favorable access to devices not on the common local bus, page 3, paragraph 0025).

As to claim 19, Hadwiger discloses the communication apparatus wherein accesses by the one or more other bus masters to the bus are restricted by terminating burst transfers early in response to the signal (The arbitration module is programmed to afford less favorable access to devices not on the common local bus, page 3, paragraph 0025).

As to claim 20, Shaeffer discloses the communication apparatus wherein the signal indicative of a change of mode of operation of the RF circuit is generated in response to execution of a software instruction (Figure 6 illustrates mode selection under software control, COL. 9, lines 7 - 15).

As to claim 22, Hadwiger discloses the method wherein accesses by the one or more bus masters are restricted by implementing a less favorable arbitration policy for the one or more bus masters in response to the signal (Figure 3 illustrates an arbiter 211 that comprises three arbiters, namely 314,315, and 316. The programmable arbitration priority is set dependent on the bandwidth requirement of subsystem. The system comprises of 15 programmable slots in a round robin-table. System that is at the bottom of the programmable slots would have a less favorable arbitration policy, COL. 9, lines 1 – 30).

As to claim 47, Shaeffer discloses the communication apparatus wherein the interrupt service routine performs functionality to prepare the digital processing circuit for a shutdown mode of the digital processing circuit (Figure 6 illustrates control circuitry to perform said function, Col. 9, lines 7 - 15).

As to claims 50, and 54, Hadwiger discloses the mobile phone and communication apparatus wherein the first bus master is provided exclusive access to the bus during the second period of operation (Granting bus access by various modules, COL. 3, lines 23 - 40).

As to claim 32, Shaeffer/Hadwiger discloses a mobile phone comprising: a radio frequency (RF) front-end circuit for operating on a radio frequency signal;

Shaeffer teaches a digital processing circuit coupled to the RF front-end circuit, wherein the digital processing circuit includes a first bus master coupled to a bus and one or more other bus masters coupled to the bus (Figure 1 illustrates RF circuit 114 coupled to bus master 116); and

Hadwiger teaches a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters (first bus master and the one or more other bus masters as system illustrated in figure 2 comprises multiples bus masters such as 201 and 202 with arbiter 211 that configures the common bus access between said masters, (page 1, paragraph 0010);

Shaeffer teaches wherein accesses by the one or more other bus masters to the bus

are restricted in response to a signal indicative of a change in a mode of operation of the RF front-end circuit (Time controller 110 is access controller to prevent noise coupling between the analog and digital circuitry, COL. 6, lines 1 - 10); and wherein the RF front-end circuit and the digital processing circuit are fabricated on a single integrated circuit chip (Single chip embodiment, COL. 11, lines 23 – 27).

As to claim 33, Shaeffer discloses the mobile phone wherein the signal is indicative of a change to an active mode of operation of the RF front-end circuit (Figure 1 illustrates an interrupt signal 18 used to indicate the active mode of the RF circuit, Col. 2, lines 9 – 18).

As to claim 48, Shaeffer discloses the communication apparatus as recited in claim 42 wherein the RF circuit and the digital processing circuit are integrated on a single chip (SOC solution that integrates RF circuits and digital circuits on the same piece of silicon, COL. 11, lines 23 – 27).

(10) Response to Argument

In response to the Appellant's argument with respect to the question raised under ***35 USC § 103*** rejection of claims 1-41, and 49-56 in the Appeal brief, the examiner disagrees.

In the Appeal brief, the Appellant argues that" the Examiner does not address restricting issued (e.g., by a bus master) access requests as in the claimed

invention. Aspects of Appellant's claimed invention allow for a bus master to continue operating while, for example, running a transition interrupt procedure (see, e.g., Appellant's Specification at paragraphs 35-41). In some implementations, other bus masters continue to operate and therefore may issue access requests; the AHB bus is capable of restricting those access requests. Thus, there is a clear (and often important) differentiation between restricting an 'issued access request' and shutting down a bus master so that no requests issue. Claims 1-41 and 49-56 each include aspects directed to restricting issued access requests. This is in contrast to the Examiner's asserted combination, which would restrict accesses only to the extent that requests are prevented from ever issuing."

In response, the Examiner presents the following response. In examining the Appellant's Specification at paragraphs 35-41, the definition of restricting access requests is described. In particular Figure 4B, and paragraph 41 details said definition. As stating that restrict access signal insertion ***may cause*** (emphasis added) other bus master activity to be terminated. ***This does not preclude the processor being fully terminated to meet the stated limitation.*** Prior art, Shaeffer teaches in Figure 2 of the time controller 210 coupled to processor 216. Signal of time controller 210 provides needed clocking to processor 216. Without said stimulus, the processor 216 will be terminated, and thus access is restricted by unselected master, COL. 5, line 63 - COL. 6, line 32. Figure 7 is illustrative of the restriction of signal. When, analog signal is on, the digital logic is terminated to eliminate noise injection into sensitive analog portion. Thus prior art meets the breadth and scope of the claimed limitation.

Further, the Appellant argues that the Examiner has provided insufficient details as to how the elements of the prior art are combined. **The crafted combination of elements by Appellant as illustrated in figure 2, page 10 is incorrect.** The Examiner points to the following description of combining the elements of both references. Figure 2 of Hadwiger illustrates the mega blocks that comprise a multi-processor system. The following table illustrates the elements as mapped to application.

Application Element	**Shaeffer Contribution**	**Hadwiger Contribution**
First bus master	Figure 2, processor 216	
One or other bus master		Fig. 3, MCU, 307
Bus arbiter		Fig. 3, with (bus arbitration unit) BAM arbiter 211
Signal indicating mode change of RF circuit	Fig. 2, Time controller 210 detailed, Said controller regulates the operation via clock signal of processor 216	Fig. 3, with Timing controller macro 311

Hadwiger comprises the multi masters, and arbiter. In addition, the peripheral subsystem 311 comprises a generic timing controller affords coupling of peripherals to on chip processors, COL. 4, lines 39-40. The Shaeffer reference provides the detailed circuitry of time controller that fleshes out operation of said element. Thus Figure 3

below illustrates the elements with the Shaeffer reference providing the timing controller 311 macro details.

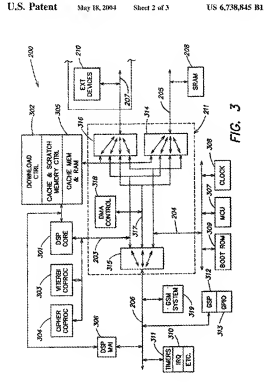

Figure 3 of Hadwiger illustrates a device comprising a plurality of processor macros, arbiters, and specifically timer 311. Said timer controls the system timing, interrupt, and set and clear connections to the device 200. Thus it would be reasonable for one of ordinary skill in the art to combine the timing control features of Shaeffer and Hadwiger to provide a system with multiple processors that need support modules to be arbitrated properly, COL. 1, lines 24 - 41. The reasonable combination of the teachings is thus clear.

Further, the Appellant has argued that" It should be apparent that 1) when deactivated by time controller 110, DSP 116 would not issue any requests, and 2) arbitration decisions of BAM 211 are not responsive to time controller 110. The following discussion explains why the aforementioned elements are relevant to the lack of correspondence between the asserted combination and the claimed invention. Appellant respectfully submits that the Examiner's definition of restriction, which states that in the prior art "no access requests would be generated, and thus, there would be no access requests to restrict," does not address Appellant's previous arguments (see also, Appellant's Responses dated February 20, 2008 and July 25, 2007, both of which are incorporated by reference in their entirely). Thus, the Examiner has explicitly stated that the combination restricts access requests by preventing issuance/generation thereof (i.e., no access requests are issued); however, various claim limitations are directed to restricting issued (past tense) requests. Thus, the claim limitations are directed to restriction of a request that has been issued. Correspondence to such limitations cannot be shown by simply preventing an access request from issuing because the limitations require that the access request actually issues. In the Advisory Action, the Examiner states that Appellant's "specification provides no limiting definition for restricting, therefore the examiner is may interpret broadly the meaning of said term." Once again the Examiner continues to focus on the meaning of the word "restricting" instead of on what the claim limitations require to be restricted (i. e., issued access requests). As such, the Examiner's asserted combination does not correspond to the claimed invention because no access requests are issued and thus the asserted

combination does not restrict issued requests. Accordingly, the cited combination does not correspond to the claimed invention. For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claims 1-41 and 49-56 fails, and therefore must be reversed."

In response to Appellant's argument, the Examiner points to the exact language of the limitation.

wherein accesses requests issued by the one or more other bus masters to access the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF circuit.

First, let's examine the specification's definition of restricting access. Figure 4B, and paragraph 41 of the specification, details said definition. As stating that restrict access signal insertion ***may cause*** (emphasis added) other bus master activity to be terminated. ***This does not preclude the processor being fully terminated to meet the stated limitation.***

The timing controller 110 of Shaeffer comprises a programmable delay locked loop. This affords the clocking capability for the digital masters to be terminated as illustrated in Figure 7. When the analog portion is on, the digital circuitry is off, and thus restricted. The plain meaning of the term is in use, and the applicant has not provided any limiting definition upon which to interpret the claim. Thus the applied definition means to bounds and means of the claim, and said interpretation is reasonable.

With regards to the Appellant's argument with respect to claims 42-48, "More other bus masters an response to a signal indicated a change to an active mode of operation. With particular regard to claims 42-48, Appellant submits that the Examiner's response fails to show correspondence to a bus arbiter that implements a less favorable arbitration policy. Neither reference alone nor in combination teaches or suggests a bus arbiter that implements a less favorable arbitration policy. Instead, the Shaeffer reference teaches powering down the processor, while the Hadwiger reference teaches a bus arbiter. As the Examiner's response merely identifies elements of the Shaeffer and Hadwiger references (i. e., a shut down signal and an arbiter), there is no support in the record for a modification to the arbiter of Hadwiger. Instead, as asserted by the Examiner's response, the combination prevents issuance of access requests using the power down function of the Shaeffer reference, whereas the arbiter of the Hadwiger reference would not restrict access requests because the Examiner has explicitly stated that they are never issued/generated. Put another way, Hadwiger appears to teach that the arbiter maintains the same arbitration policy and the Shaeffer reference does not teach or suggest modifying an arbiter. Thus, regardless of whether the processor is powered down as taught by Shaeffer, the arbiter maintains the same arbitration policy. As the arbiter of Hadwiger neither 1) responds to any signal indicating a change to an active mode, nor 2) implements a less favorable arbitration policy, the cited combination fails to correspond to the claimed invention."

The Examiner disagrees, and point to the following teaching of Hadwiger. Figure 3 illustrates an arbiter 211 that comprises three arbiters, namely 314,315, and 316. The

programmable arbitration priority is set dependent on the bandwidth requirement of the plurality of subsystems. The arbitration scheme comprises of 15 programmable slots in a round robin-table. Modules with less bandwidth capability that is at the bottom of the programmable slots would have a less favorable arbitration policy, COL. 9, lines 1 – 30. The prior art clearly teaches the limitation of less favorable arbitration policy, relative to the highest priority of the higher bandwidth modules.

Finally, the Appellant argues that "There are many reasons why the Examiner is required to particularly identify and analyze an assertion combination. For example, to establish a prima facie case of obviousness the Examiner must provide a reason to combine the elements. Appellant respectfully submits that the specifics of how the asserted elements would function together are necessary to 1)judge whether the combination (not just the individual elements) in fact corresponds to the claimed invention and 2) determine whether a proper reason to combine the elements exists. As the record, including the cited references and the Examiner's response, is deficient regarding support for such details, Appellant submits the rejections are improper and cannot stand.

The Examiner disagrees. The Examiner points to the following teaching of Hadwiger as motivation for combining said references. One of ordinary skill in the art would have been motivated to modify the processor of Shaeffer with the multiple processor core of Hadwiger to provide a cost effective solution for mobile phones that requires multiple processors and analog circuitry, COL. 1, lines 25 - 40. Therefore, the applicant's argument is not considered persuasive.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Thus, in response to the appeal brief filed on 06/30/2008, for the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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